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John A. Jordan
11 Hyspot Road
Greenfield Center, NY 12833

EXAMINER	
SEMENENKO, YURIY	

ART UNIT	PAPER NUMBER
2841	

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Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No.	Applicant(s)	
	10/722,226	AUDET ET AL.	
	Examiner	Art Unit	
	Yuriy Semenenko	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) *10-18 and 22-30* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 19-21* is/are rejected.

7)☒ Claim(s) *11-18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/25/03page 1*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 11-18 are objected to because of the following:
Examiner notes that claims 11-18 describe a multilayer chip carrier which lacks proper antecedent basis, because these claims depend on claim 10 which describes a multilayer chip substrate. Examiner called Mr. J. Jordan on November 9, 2005 to clarify subject matter of this claims. Mr. Jordon confirmed that claims 11-18 should be --a multilayer chip substrate--. To eliminate any discrepancy Mr. J. Jordan must change the text of the claims 11-18 to recite – a multilayer chip substrate--.

Election/Restrictions

2.1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-9 and 19-21 drawn to a multilayer chip carrier, classified in class 174 subclass 260.

II. Claims 10-18 drawn to a multilayer chip carrier substrate, classified in class 174 subclass 260.

III. Claims 22-30 drawn to a method of fanout redistribution of signal pads on multilayer chip carrier, classified in class 29 subclass 825.

The inventions are distinct, each from the other because of the following reasons:
2.2 Inventions III and I, II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case product as claimed can be made by another

and materially different process. For example, product could be made by a method wherein the plurality of signal pads are not arranged adjacent a plurality of power distribution busses.

2.3. Inventions group I and group II are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because combination (a multilayer chip carrier) may work without subcombination (a multilayer chip carrier substrate) as claimed in claim 10-18 but instead of using a multilayer chip carrier substrate without a third set of signal pads. The subcombination (a multilayer chip carrier substrate) has separate utility such as in assemblies where a number of subassemblies are stacked one on top of another.

2.4. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, and the search required for Group I and II is not required for Group III, restriction for examination purposes as indicated is proper.

2.5. During a telephone conversation with J. A. Jordan (Reg. No. 24655) on November 9, 2005, a provisional election with traverse was made to prosecute the invention of group I, to a multilayer chip carrier, Claims 1-9 and 19-21. Affirmation of this election must be made by applicant in replying to this Office action. Claims 10-18 and 22-30 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Specification

3. The disclosure is objected to because of the following informalities:

page 10, line 22: there is not layer FC3 in Fig.6. Appropriate correction is required.

Claim Objections

4. Claim 1 is objected to because of the following informalities:

Claim 1 "within the footprint of at least one chip " should be changed to – within a footprint of at least one chip-- for proper antecedence basis.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5.1. Claims 1,2, 8, 9 and 19-21 are rejected under 35U.S.C. 103(a) as being obvious over Admitted by Applicant (Prior Art, hereinafter "APA") in view of Lin (Patent # 5258648 hereafter "Lin") .

5.1.1. Regarding claim 1: APA discloses in Fig. 1 a multilayer chip carrier, comprising: a layer of dielectric material FC3, Fig. 4 and Specification, page 8, line 25 having a plurality of signal pads 37, Fig. 4 formed thereon in a pattern of signal pads related to a pattern of signal pads within the footprint of at least one chip 7, Fig. 1, to be carried on said chip carrier, said plurality of signal pads including a first set of signal pads near the edge of said chip footprint 37a, 37b, 37c , Fig. 4 each having a conductive line 39 connected thereto extending beyond the edge 23 of said chip footprint and a second set of signal pads 37,

except APA doesn't explicitly teach set of signal pads each having a conductive line connected thereto extending to connect to respective signal pads positioned nearer the said edge of said chip footprint.

Lin discloses in Fig.1 set of signal pads 24 each having a conductive line 26 connected thereto extending to connect to respective signal pads 27 positioned nearer the said edge of said chip footprint. [For connection with conductive line 26 vias 24 have to have pads on its, Fig. 5 or vias 24 connected to bump 16 directly Fig. 4.] At time the invention was made, it was well know to use signal pads each having a conductive line connected thereto extending to connect to respective signal pads positioned nearer the said edge of said chip footprint.

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for APA to include in his invention that set of signal pads each having a conductive line connected thereto extending to connect to respective signal pads positioned nearer the said edge of said chip footprint to provide options for signal contact escape.

5.1.2. Regarding claim 2: APA discloses in Fig. 1 the multilayer chip carrier having all of the claimed features as discussed above with respect claim 1,

except APA doesn't explicitly teach at least some of said signal pads on said dielectric layer nearer the said edge of said chip footprint have a conductive via

connected thereto that form a set of conductive vias that extend through said layer of dielectric material to the opposing surface thereof.

Lin discloses in Fig.1 at least some of said signal pads 14 on said dielectric layer nearer the said edge of said chip footprint have a conductive via 24, Fig. 4, connected thereto that form a set of conductive vias that extend through said layer of dielectric material to the opposing surface thereof. At time the invention was made, it was well know to use at least some of said signal pads on said dielectric layer nearer the said edge of said chip footprint have a conductive via connected thereto that form a set of conductive vias that extend through said layer of dielectric material to the opposing surface thereof.

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for APA to include in his invention that at least some of said signal pads on said dielectric layer nearer the said edge of said chip footprint have a conductive via connected thereto that form a set of conductive vias that extend through said layer of dielectric material to the opposing surface thereof to provide options for signal contact escape.

5.1.3. Regarding claim 8: APA discloses in Fig. 1 the multilayer chip carrier having all of the claimed features as discussed above with respect claim 1, including a chip 7, attached thereto, Fig. 1.

5.1.4. Regarding claim 9: APA discloses in Fig. 1 the multilayer chip carrier having all of the claimed features as discussed above with respect claim 8, wherein said multilayer chip carrier is electrically attached to a printed wiring board 17, Fig. 1.

5.1.5. Regarding claim 19: APA discloses in Fig. 1 a multilayer chip carrier, comprising: a first layer FC3, Fig. 4 of dielectric material (Specification, page 8, line 25) having a plurality of signal pads 37 formed thereon arranged in a pattern of signal pads related to signal pads within the footprint of at least one chip 7, Fig. 1 to be carried by said chip carrier, said plurality of signal pads including a first set signal pads near the

edge of said chip footprint 37a, 37b, 37c, Fig. 4 each having conductive lines 39 connected thereto extending beyond the edge 23 of said chip footprint and a second set of signal pads 37, a second layer FC2, Fig. 5 of dielectric material having a set of signal pads 37 arranged thereon respectively connected to said conductive vias 41 extending through said first layer of dielectric material FC3, and a third layer FC1, Fig.6 of dielectric material having a set of signal pads 37 arranged thereon respectively connected to the said conductive vias 37 on the FC2 layer of Fig. 5 extending through said second layer of dielectric material (Specification, page 10, line 19-23) and having conductive lines 39, Fig. 6 respectively connected thereto extending beyond the edge 23 of said chip footprint,

except APA doesn't explicitly teach set of signal pads each having a conductive line connected thereto extending to connect to respective signal pads positioned closer the said edge of said chip footprint with said signal pads positioned closer to the edge of said chip footprint having conductive vias connected thereto extending through said first layer of dielectric material.

Lin discloses in Fig.1 set of signal pads 24 each having a conductive line 26 connected thereto extending to connect to respective signal pads 27 positioned closer the said edge of said chip footprint. [for connection with conductive line 26 vias 24 have to have pads on its, Fig. 5 or vias 24 connected to bump 16 directly Fig. 4.] with said signal pads 14, Fig. 1, positioned closer to the edge of said chip footprint having conductive vias 24, Fig. 2, connected thereto extending through said first layer of dielectric material. At time the invention was made, it was well know to use set of signal pads as claimed in claim 19, first paragraph.

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for APA to include in his invention that a second set of signal pads each having a conductive line connected thereto extending to connect to respective signal pads positioned closer to the edge of said chip footprint with said signal pads positioned closer to the edge of said chip footprint having conductive vias connected thereto extending through said first layer of dielectric material to provide options for signal contact escape.

APA also doesn't explicitly teach this set of signal pads having respective conductive lines connected thereto extending to respectively connect to further signal pads positioned closer to the edge of said chip footprint, said further signal pad having conductive vias connected thereto extending through said second layer of dielectric material.

Lin discloses in Fig.1 set of signal pads 24 having respective conductive lines 26 connected thereto extending to respectively connect to further signal pads 27 positioned closer to the edge of said chip footprint, said further signal pad having conductive vias 24, Fig. 2, connected thereto extending through said second layer of dielectric material. This structure for second layer is the same as claimed in claim 19, first paragraph for first layer of dielectric material, as discussed above. And further, It has been held that a mere duplication of parts, absent new or unexpected results, is within the level of ordinary skill. In re Harza, 274 F.2d 669, 124 USPQ 378 (CCPA 1960). Therefore, at time the invention was made, it was well know to use set of signal pads as claimed in claim 19, second paragraph.

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for APA to include in his invention that another set of signal pads having respective conductive lines connected thereto extending to respectively connect to further signal pads positioned closer to the edge of said chip footprint, said further signal pad having conductive vias connected thereto extending through said second layer of dielectric material to provide options for signal contact escape.

5.1.6. Regarding claim 20: APA, as modified, discloses the multilayer chip carrier having all of the claimed features as discussed above with respect claim 19, including at least one chip 7, Fig. 1 having a pattern of electrical contacts corresponding to said pattern of signal pads electrically connected thereto.

5.1.7. Regarding claim 21: APA, as modified, discloses the multilayer chip carrier having all of the claimed features as discussed above with respect claim 20, wherein said chip carrier 7, Fig. 1, is electrically attached to a printed wiring board 17.

5.2. Claims 3-7 are rejected under 35U.S.C. 103(a) as being obvious over Admitted by Applicant (Prior Art, hereinafter "APA") in view of Lin and in view of Arima et al. (Patent #6479758 hereinafter "Arima").

5.2.1. Regarding claim 3: APA discloses in Fig. 1 the multilayer chip carrier having all of the claimed features as discussed above with respect claim 2, including a further layer of dielectric material beneath said layer of dielectric material having signal pads, 37 and 37A thereon (FC 2 Layer, Fig. 5),

except APA doesn't explicitly teach respective ones of said signal pads connected to respective ones of said conductive vias of said set of conductive vias.

Aruma discloses in Fig. 2 respective ones of said signal pads 4a connected to respective ones of said conductive vias 18a of said set of conductive vias. At time the invention was made, it was well know to use respective ones of said signal pads connected to respective ones of said conductive vias of said set of conductive vias.

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for APA to include in his invention that respective ones of said signal pads connected to respective ones of said conductive vias of said set of conductive vias to provide escape of the signal contact.

5.2.2. Regarding claim 4: APA discloses in Fig. 1 the multilayer chip carrier having all of the claimed features as discussed above with respect claim 3, wherein at least some of said signal pads on said further layer of dielectric material each have a conductive line connected thereto extending to connect to respective further signal pads nearer the edge of said chip footprint. This structure for further layer exactly the same as claimed in claim 1 for layer of dielectric material, as discussed above with respect claim 1. And further, It has been held that a mere duplication of parts, absent new or unexpected results, is within the level of ordinary skill. In re Harza, 274 F.2d 669, 124 USPQ 378 (CCPA 1960).

5.2.3. Regarding claim 5: APA, as modified, discloses the multilayer chip carrier having all of the claimed features as discussed above with respect claim 4, wherein at least some of said further signal pads 37 Fig. 5 have conductive vias connected thereto that extend through said further layer of dielectric material to connect to signal pads on another layer of dielectric material (Specification, page 10, lines 19-23) with said signal pads 37, Fig. 6, on said another layer of dielectric material having conductive lines 39 connected thereto extending beyond the edge of said chip footprint (Fig. 6).

5.2.4. Regarding claim 6: APA, as modified, discloses the multilayer chip carrier having all of the claimed features as discussed above with respect claim 5, wherein said plurality of signal pads 37, Fig. 4 are arranged adjacent a plurality of power distribution busses 35.

5.2.5. Regarding claim 7: APA, as modified, discloses the multilayer chip carrier having all of the claimed features as discussed above with respect claim 6, wherein power PTHs 43are connected to said power distribution busses 35 in the region of said signal pads 37.

Relevant Art

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

6.1. Daves et al. (Patent # 6974722) teaches a structure for translating wiring connections from points in a first grid to corresponding points in a second grid in a chip carrier module is disclosed. In an exemplary embodiment, the structure includes a first translation layer, coupled to the first grid, the first translation layer translating the first grid in an x-axis direction. A second translation layer is coupled to the first translation layer, the second translation layer for translating said wiring connections from the first

grid in a y-axis direction, the y-axis direction being orthogonal to the x-axis direction. The second translation layer is further coupled to the second grid.

6.2. Yamada et al. (Patent # 6548907) teaches a semiconductor device includes a semiconductor chip carrying a plurality of contact electrodes on a principal surface.

7.1. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yuriy Semenenko whose telephone number is (571) 272-6106. The examiner can normally be reached on 8:30am - 5:00pm.

7.2. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571)- 272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

7.3. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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KAMAND CUNEO
SPE 2841